~~S2037~~

# METHOD FOR FABRICATING A SEMICONDUCTOR STRUCTURE

~~Description~~

## CLAIM FOR PRIORITY

This application claims the benefit of priority to German Application No. 102 55 686.5, which was filed in the German language on November 28, 2002.

## TECHNICAL FIELD OF THE INVENTION

The present invention relates to a method for fabricating a semiconductor structure.

## BACKGROUND OF THE INVENTION

Although applicable, in principle, to any desired integrated circuits, the present invention and also the problem area on which it is based are explained with regard to memory cell semiconductor structures with trench capacitors in silicon technology.

Figure 2 shows ~~a known arrangement scheme for a~~conventional memory cell semiconductor structures ~~[sic]~~ with trench capacitors in silicon technology, which is also referred to as an MINT cell layout.

In Figure 2, reference symbols G1 to G8 designate trench capacitors which are arranged offset relative to one another in pairs in rows and columns. Lying between the trench capacitors G1 to G8 are active regions AA1 to AA7 or shallow trench isolation structures STI filled with an insulation material, which enclose the active regions AA1 to AA7 in insular fashion.

Accommodated in the active regions AA1 to AA7 are respective selection transistors (not shown) for the trench capacitors G1 to G8. In this case, the selection transistors of in each case two trench capacitors, for example G4 and G5 have a common bit line terminal lying approximately in the center of the active region, in this case AA4. Situated between the bit line terminal and the respective trench capacitor is a gate line terminal connected to a respective word line. In the case of the present layout, the bit lines (not shown) run in the row direction and the word lines (not shown) run in the column direction. The cells are configured symmetrically with respect to the common bit line terminal.

Filling the isolation trench structure with the insulating filling material, which is generally composed of silicon oxide, has proved to be problematic in case of such an arrangement scheme for a memory cell semiconductor structure with trench capacitors. This is because the structures have a high aspect ratio in particular in the isolation trenches between the adjacent rows, which generally has the effect that shrink holes form in the insulating filling material. It is primarily at the location at which two adjacent active regions overlap that the aspect ratio of the STI trench to be filled is very high and the risk of shrink hole formation is thus the greatest.

Usually, ~~said~~ the shrink hole formation can only be avoided by carrying out multiple deposition and wet-chemical etching-back of the insulating filling material.

The ~~problem area on which the~~ present invention ~~is based thus consists in providing~~ provides an improved method for

fabricating such a semiconductor structure which makes it possible to reduce the risk of shrink hole formation during filling of the isolation trenches.

~~According to the invention, this problem is solved by means of the fabrication method specified in claim 1.~~

~~The a~~Advantages of the fabrication method according to the invention are, in particular, that the aspect ratio can be relaxed in the critical overlap region and regions with a particularly critical aspect ratio are eliminated or can at least be greatly reduced in size. The risk of shrink hole formation during filling of the isolation trenches is reduced from the outset in this way.

The ~~idea on which the present invention is based consists in the receding~~ process ~~resulting~~ results in reduction or elimination of an overlap region between two strip sections of adjacent rows in comparison with an overlap region which would be present without the receding process.

~~Advantageous developments and improvements of the subject matter of the invention are found in the subclaims.~~

In accordance with one preferred ~~development~~embodiment, the trenches each have a trench capacitor with a corresponding filling, which is sunk with respect to the top side of the semiconductor substrate.

In accordance with a further preferred ~~development~~embodiment, the receding process is realized by an isotropic, preferably wet-chemical, etching process, as a result of which the thickness of the hard mask that has been caused to recede is reduced in comparison with the

thickness of the hard mask. The aspect ratio can be configured even more favorably as a result.

In accordance with a further preferred ~~development~~embodiment, the first hard mask is composed of silicon nitride.

In accordance with a further preferred ~~development~~embodiment, the second hard mask is composed of silicon oxide.

In accordance with a further preferred ~~development~~embodiment, the filling material is composed of silicon oxide.

In accordance with a further preferred ~~development~~embodiment, the receding process results in complete elimination of an overlap region between two strip sections of adjacent rows.

## BRIEF DESCRIPTION OF THE DRAWINGS

Exemplary embodiments of the invention are illustrated in the drawings and explained in more detail in the description given below.

Figures 1a-f show ~~diagrammatic illustrations of~~ successive method stages of a method for fabricating a semiconductor structure as an embodiment of the present invention~~; and~~.

Figure 2 shows ~~a known arrangement scheme for a~~ conventional memory cell semiconductor structures ~~[sic]~~ with trench capacitors in silicon technology.

In figures 1a-f, identical reference symbols designate identical or functional identity constituent parts.

## DETAILED DESCRIPTION OF THE INVENTION

The embodiment illustrated in figures 1a-f relates to the known arrangement scheme explained above in accordance with figure 2.

In figure 1a, r1, r2 designate adjacent rows and s1, s2 and s3 designate adjacent columns of the memory cell arrangement, the trenches G11 and G12 being arranged in the row r1, ~~said~~ the trenches serving for trench capacitors which have no selection transistors with a common accompanying ~~[sic]~~ terminal. The trench G21 is provided in offset fashion in the row r2.

The right-hand part of figures 1a-f in each case comprises a sectional illustration along the broken line in the left-hand part.

The sectional illustration of figure 1a reveals that, in the process state considered, a mask 50 made of silicon nitride is provided on the semiconductor substrate 10 with the trenches G11, G12, G21, which mask has served for etching the trenches G11, G12, G21 by means of a corresponding silicon etching process.

As can further be seen from figure 1a, a filling made of polysilicon 20 is provided in the upper part of the trenches G11, G12, G21, said filling being sunk with respect to the top side OS of the semiconductor substrate 10. Said filling 20 is composed of polysilicon and is a part of the capacitor structure of the trench capacitor

situated in the trenches, namely a buried connection strip for the inner capacitor plate which, in a later process step, is connected to the associated selection transistor in the active region through a corresponding diffusion region.

Finally, UC in figure 1a designates an undercut region between the semiconductor substrate 10 and the hard mask 50 made of silicon nitride, where pad oxide (not shown) situated there has been undercut during the formation of the capacitor structure.

In accordance with figure 1b, in a subsequent process step, a selective wet-chemical etching-back of the silicon nitride of the hard mask 50 is effected for the purpose of forming a hard mask 50' that has been caused to recede with respect to the trench wall and whose thickness has been thinned. In this embodiment, the receding distance $\Delta$ is 40 nm to 50 nm, and the thickness in this case decreases from 140 nm to 90 nm to 100 nm. This etching-back may expediently be carried out in hot phosphoric acid.

In a subsequent process step illustrated in figure 1c, a hard mask HM made of silicon oxide is then applied and patterned lithographically on the resultant structure. Said hard mask HM serves for defining the later isolation trench structure ST, which is produced by means of a silicon etchant. The silicon semiconductor substrate 10 that is not etched in this case (cf. figure 2) later forms the so-called active regions.

As can be seen from figure 1d, the isolation trench structure ST in the semiconductor substrate 10 subdivides the hard mask 50' that has been caused to recede along the

rows r1, r2 into strip sections $50_1'$, $50_2'$ in the row r1 and $50_3'$ in the row r2, the strip sections of adjacent rows being arranged offset with respect to one another, here for example $50_1'$ and $50_3'$. The vertical connecting line V in figure 1d reveals that virtually no overlap of the strip sections $50_1'$ and $50_3'$ is present as a result of the provision of the receding region $\Delta$, as a result of which the aspect ratio at this critical location is significantly relaxed.

In a concluding process step in accordance with figure 1e, the isolation trench structure ST is then filled and planarized by means of silicon oxide as insulating filling material FI, for example by means of a high density plasma process, which can be realized without shrink hole formation on account of the reduced aspect ratio in the overlap region KB' that has been reduced in size. Repeated deposition and etching-back of the insulating filling material FI made of silicon oxide is thus unnecessary.

Figures 1e and 1f show, in a comparison, the critical overlap region KB' and KB, respectively, in the case of causing the hard mask 50 made of silicon nitride to recede and in the case where no receding process is carried out. It can clearly be discerned that the overlap region KB' in the case of the receding process is significantly smaller than the overlap region KB in the case where this step is absent.

In the case of known structures, it was possible to relax the aspect ratio in the critical overlap region KB from 4.2 to 2.9 by means of the procedure according to the invention.

Although the present invention has been described above on the basis of a preferred exemplary embodiment, it is not restricted thereto, but rather can be modified in diverse ways.

In particular, the selection of the mask and substrate materials ~~[lacuna]~~are exemplary of the arrangement thereof are only by way of example and can be varied in many different ways.

Although in the above embodiment, the process of causing the hard mask 50 made of silicon nitride to recede still leaves a small overlap region KB', this receding process could be carried out in such a way that the overlap region is completely removed.

~~Patent Claims~~What is claimed is:

## Abstract

~~The present invention provides a~~A method for fabricating a semiconductor structure ~~having the steps of:~~includes providing a semiconductor substrate ~~(10);~~, providing a plurality of trenches ~~(G11, G12; G21)~~ in the semiconductor substrate ~~(10)~~ using a first hard mask, ~~(50), which trenches are arranged offset with respect to one another in rows (r1, r2) and columns (s1, s2, s3);~~ and causing the hard mask ~~(50)~~ to recede by a predetermined distance ~~(A)~~ with respect to the trench wall at the top side ~~(OS)~~ of the semiconductor substrate ~~(10)~~ for ~~the purpose of~~ forming a first hard mask ~~(50')~~ that has been caused to recede~~;~~. ~~providing an~~An isolation trench structure ~~(ST)~~ is provided in the semiconductor substrate ~~(10)~~ using a second hard mask ~~(HM)~~, the isolation trench structure ~~(ST)~~ subdividing the first first ~~[sic]~~ hard mask ~~(50')~~ that has been caused to recede along ~~the~~ rows ~~(r1, r2)~~ into strip sections ~~($50_1'$, $50_2'$; $50_3'$)~~ and the strip sections ~~($50_1'$; $50_3'$)~~ of adjacent rows ~~(r1, r2)~~ being arranged offset with respect to one another~~;~~. ~~t~~The receding process ~~resulting~~ results in a reduction of an overlap region ~~(KB')~~ between two strip sections ~~($50_1'$; $50_3'$)~~ of adjacent rows ~~(r1, r2)~~ in comparison with an overlap region ~~(KB)~~ which would be present without the receding process~~;~~. ~~removing the~~The second hard mask ~~(HM);~~ is removed ~~and filling and planarizing~~ the isolation trench structure ~~(ST)~~ is filled and planarized with a filling material ~~(FI)~~ using the first hard mask ~~(50')~~ subdivided into the strip sections ~~($50_1'$, $50_2'$; $50_3'$)~~.

~~Figure 1c~~

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List of reference symbols

| | |
|---|---|
| G1-G8 | Trench capacitors |
| AA1-7 | Active regions |
| STI | Shallow trench isolation |
| r1, r2 | Rows |
| s1, s2, s3 | Columns |
| 10 | Si semiconductor substrate |
| 20 | Polysilicon filling |
| OS | Top side |
| G11, G12, G21 | Trench |
| UC | Undercut region |
| V | Connecting line |
| Δ | Receding distance |
| 50, 50' | Silicon nitride hard mask |
| HM | Hard mask made of silicon oxide |
| ST | Isolation trench structure |
| $50_1$', $50_2$', $50_3$' | Strip sections |
| FI | Insulating filling material made of silicon oxide |
| KB | Overlap region |
| KB' | Reduced overlap region |

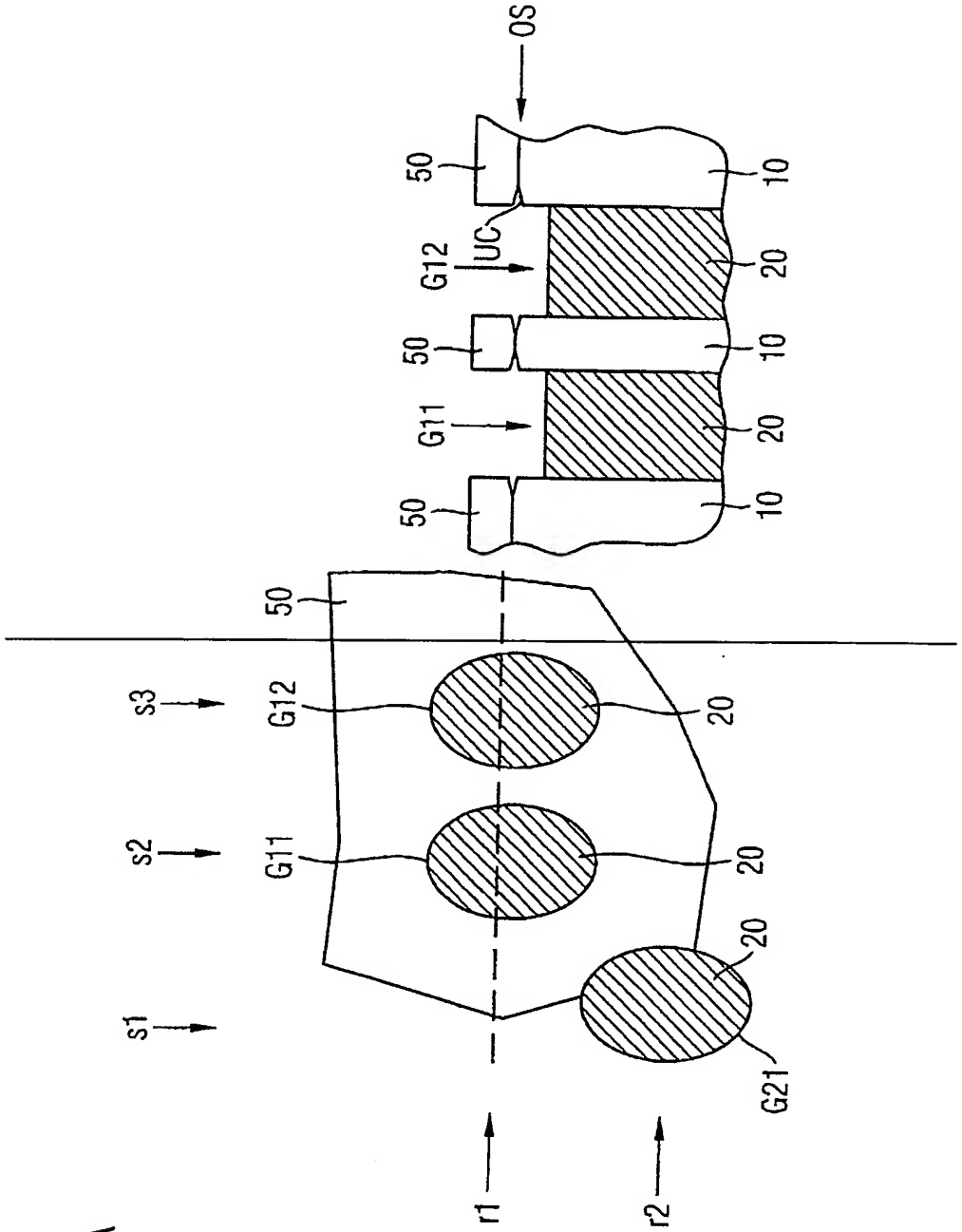
OS
50
10
G12
UC
20
50
10
G11
20
50
10
50
s3
G12
20
s2
G11
20
20
s1
G21
r1
r2

FIG 1A

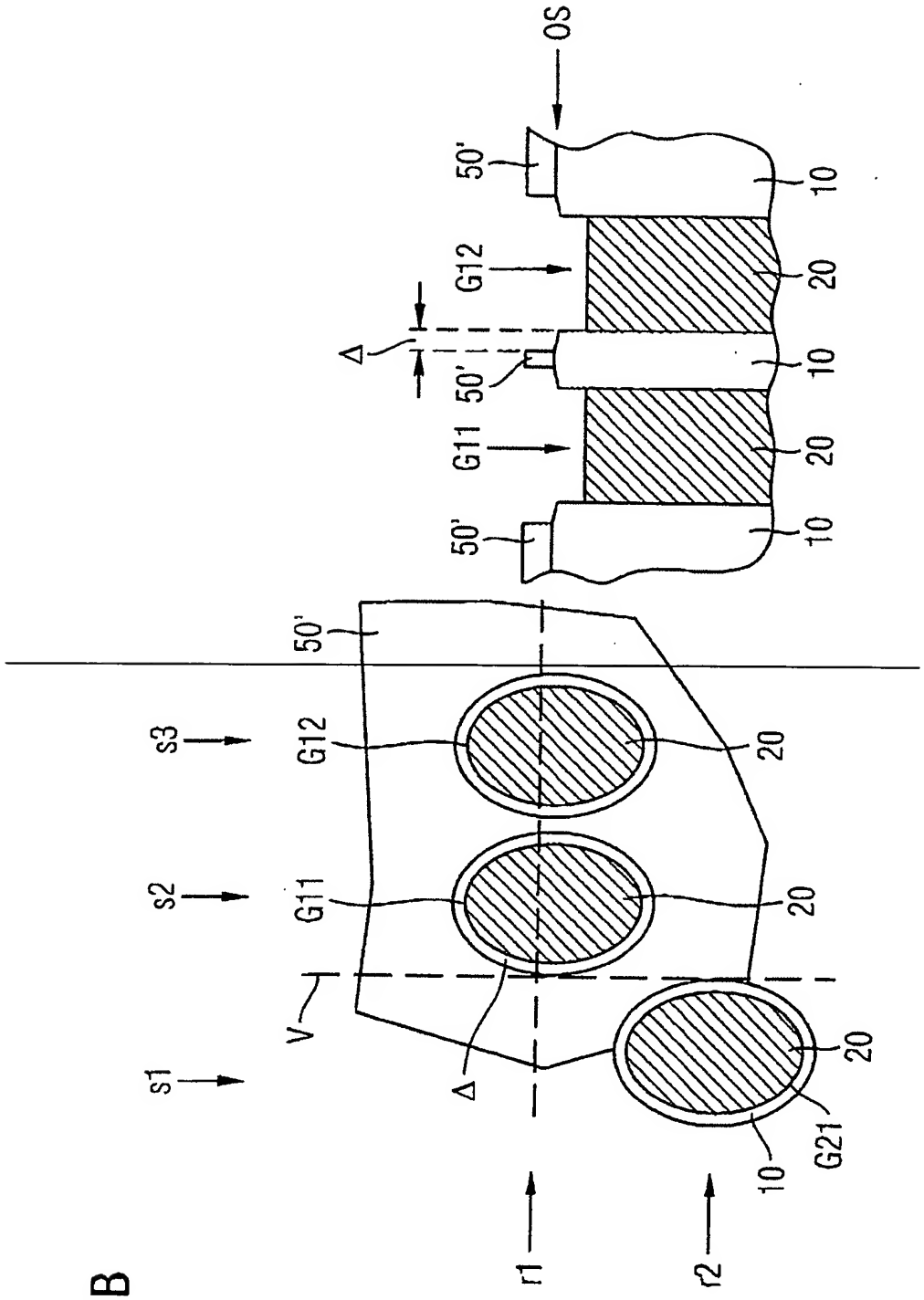
OS
50'
10
G12
20
Δ
50'
10
G11
20
50'
10
50'
s3
G12
20
s2
G11
20
V
s1
Δ
20
G21
10
r1
r2

FIG 1B

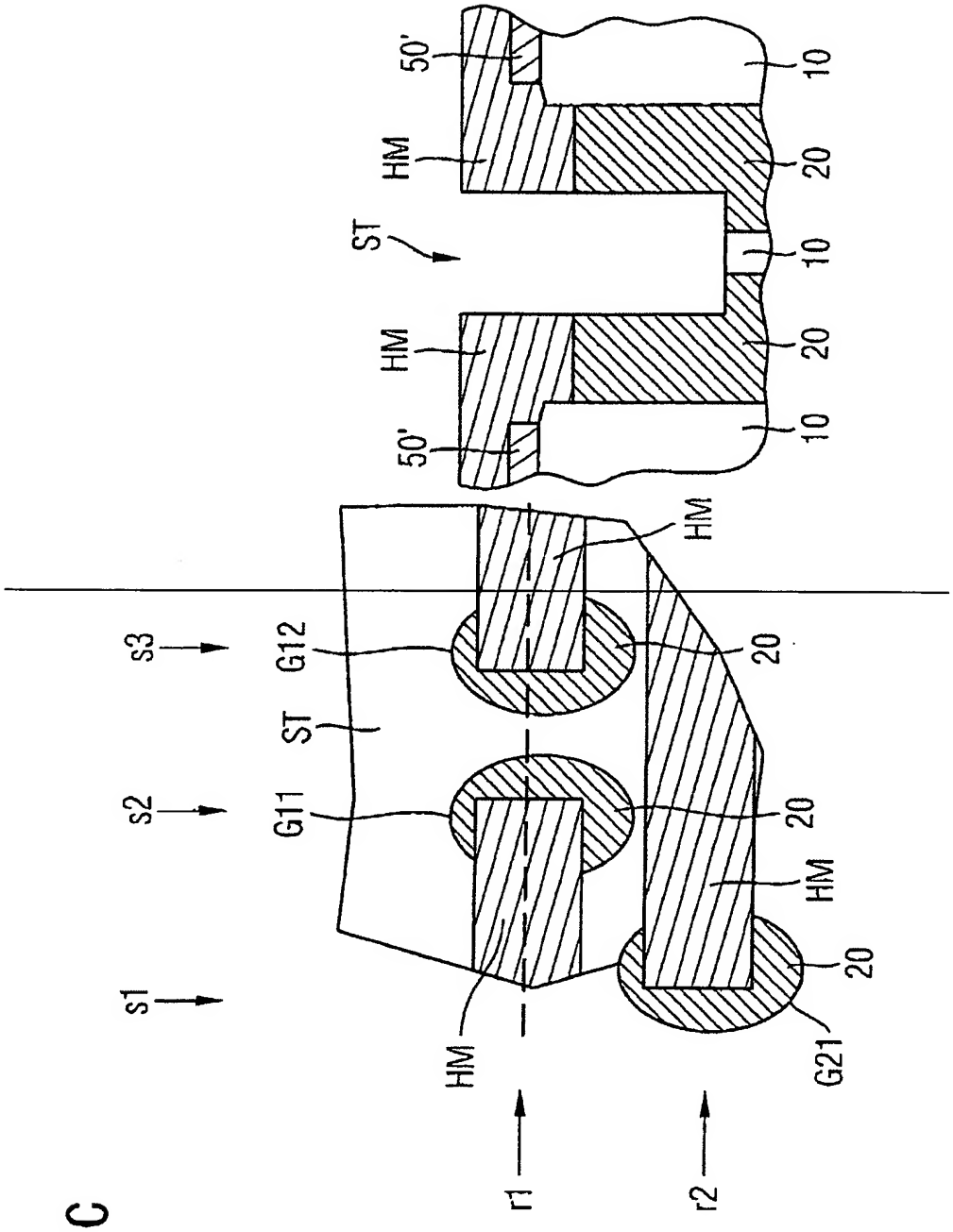
50'
HM
ST
HM
50'
10
20
10
20
10
HM
s3
G12
ST
s2
G11
s1
HM
20
20
HM
20
G21
r1
r2

FIG 1C

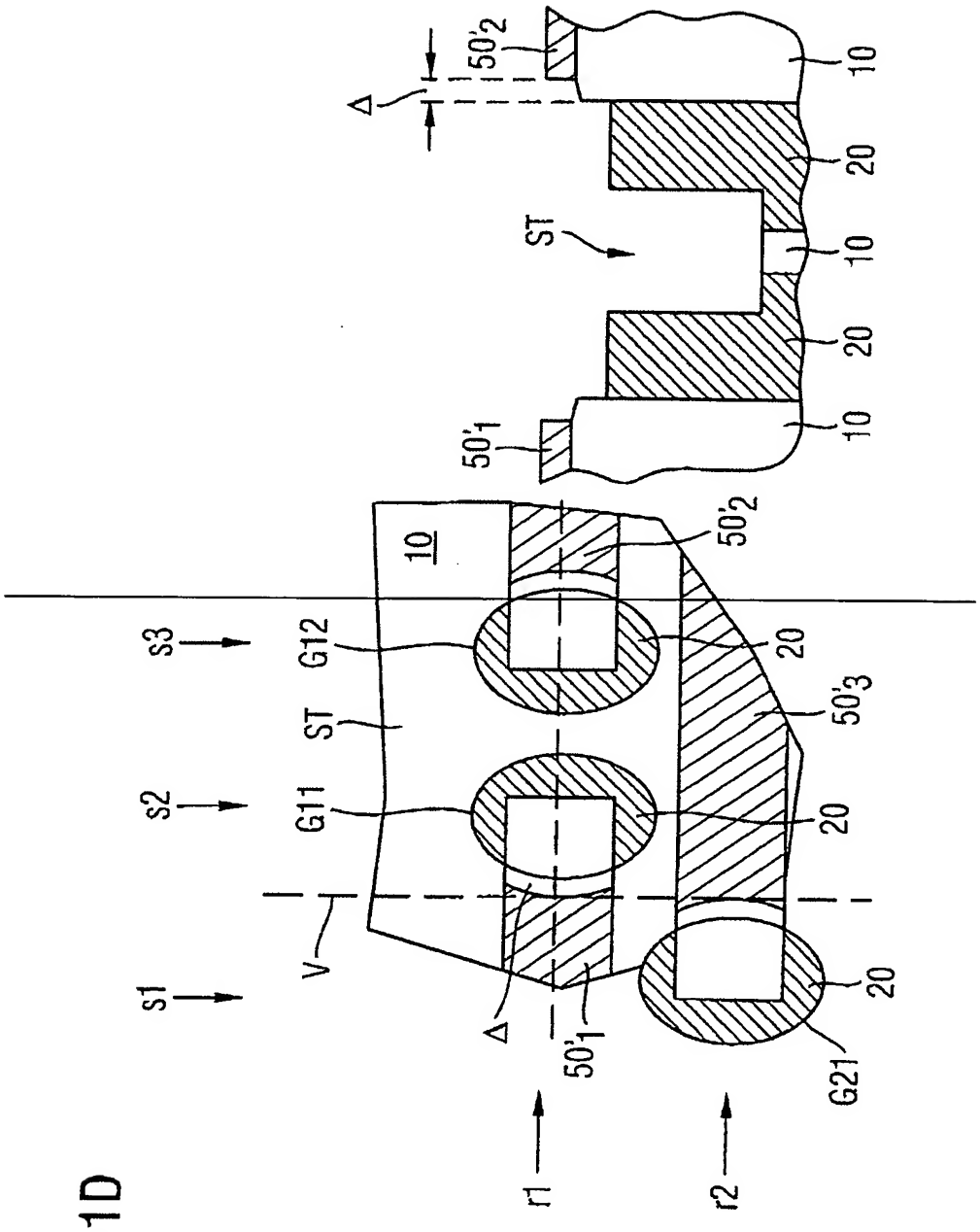


FIG 1D

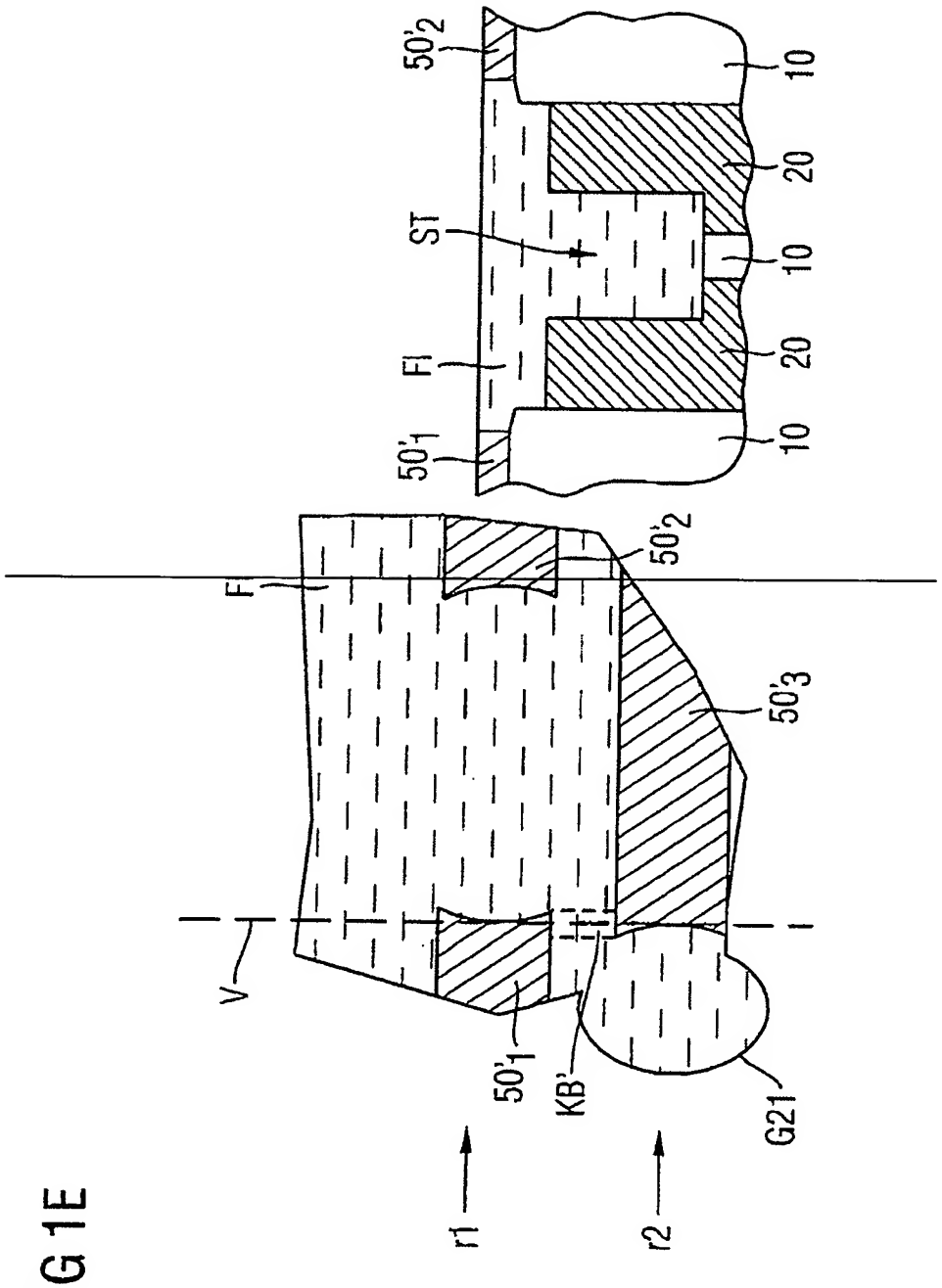


FIG 1E

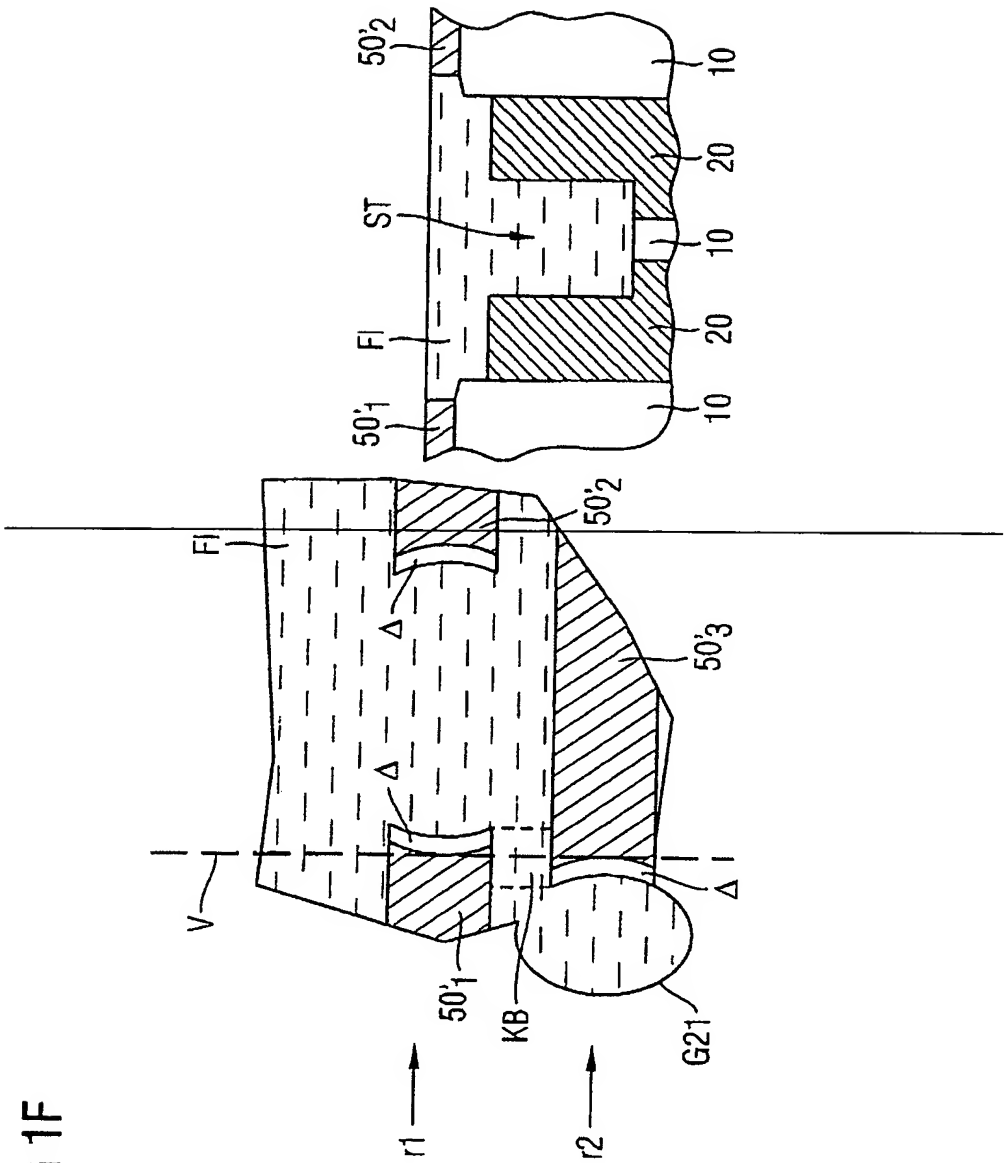


FIG 1F

FIG 2